A Hardware/Software Platform for Real-time Ethernet Cluster Simulation in OMNeT++

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Abstract

Cluster simulation is a popular method for supporting system integration in various distributed applications by simulating the environment of a subsystem under test. We contribute a scheme for cluster simulation of real-time Ethernet (RTEthernet) based distributed systems. It relies on the discrete event-based simulation framework OMNeT++, interconnected with an ARM-based co-processor. The results show that the timing requirements for the cluster simulation of small RTEthernet networks can be achieved.

Concept

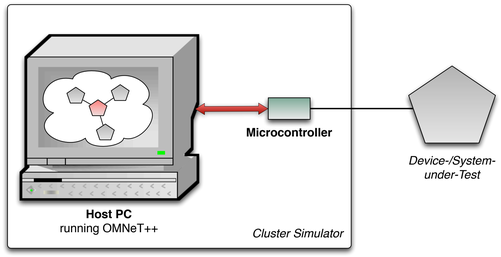

Fig. 1: Cluster simulation concept with a host PC and a dedicated microcontroller

Architecture

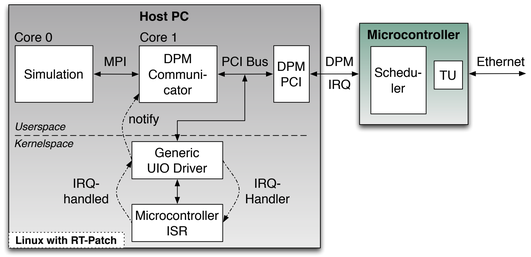

Fig. 2: Architecture with virtual dual port memory and the Message Passing Interface

Discussion of Results

- The latency of the frame reception from the real network to the simulation is linear, dependent on the frame size and has a static part of 186.4 µs
- Jitter analysis shows that incoming TT-messages have a maximum of 37 µs which is caused by the host system due to the used off-the-shelf hardware
- Applications that have latency requirements up to 230 µs can be simulated with our approach

Introduction & Motivation

- Software simulation of distributed real-time systems is established for design and reconfiguration phases
- Cluster simulation is useful by simulating not available hardware during integration and setup phases
- Environments for cluster simulation generally use dedicated and expensive real-time hardware platforms
- These platforms are inflexible and specifically designed for one use-case and do not allow modifications of the network protocol itself

Background

- A cluster simulator is only connected to the system-under-test (SUT) via the communication interface and is triggered with regular data frames
- Behavior verification of the SUT is possible on the abstract data level by analyzing the received frames
- TTEthernet [3] is a RTEthernet implementation that classifies the traffic into time-triggered (TT), rate-constrained (RC) and best-effort (BE) messages
- A fail-safe time synchronisation protocol accomplishes the required system wide time base for time-triggered transmission

Implementation

- Virtual dual port memory (DPM) connects the host with the microcontroller
- The simulation environment is separated on two dedicated CPU cores that communicate via the Message Passing Interface (MPI)
- To minimise latency and jitter the Linux real-time Kernel patch is utilised
- The Linux network stack does not fulfill the timing requirements for precise frame transmission and reception in the lower microseconds range
- Sending frames is accomplished with the high-resolution scheduler of the microcontroller
- The reception of frames in the simulation has to be prioritised due the TTEthernet message classes

Outlook

- The microcontroller is planned to be replaced by a special network interface card with a hardware time stamping unit and a higher bandwidth
- A further investigation on how the simulation can benefit from multicore parallelisation will be applied
- The utilised real-time Kernel patch and other Linux real-time approaches will be deeper analysed to reduce the jitter

Measurement Results

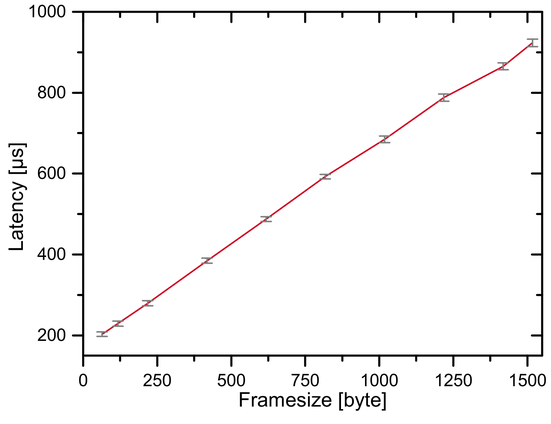

Fig. 3: Latency with standard deviation

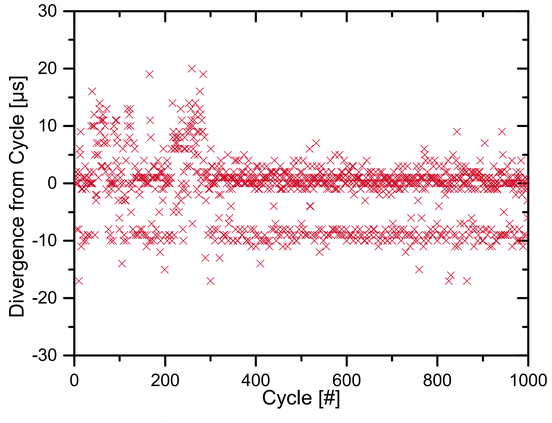

Fig. 4: Jitter distribution

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